

REMARKS

Claims 1-7 are pending. Claims 1 and 5 have been amended. No new matter has been added to the specification by these amendments.

103 Rejections

Claim 1-4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lim (6,265,265) view of The Background of the Invention. Applicants have reviewed the cited reference and respectfully submit that the present invention as recited in claim 1 is neither shown nor suggested by Lim (6,265,265) view of The Background of the Invention.

The examiner is respectfully directed to independent claim 1 which recites that an embodiment of the present invention is directed to a method for manufacturing a flash memory device having a lightly doped source region comprising:

- a) forming multiple gates on a substrate defining drain regions and source regions associated with each of the multiple gates; b) forming a first source mask exposing the source regions and portions of the gates; c) implanting the exposed source regions with n dopant ions; d) removing the first source mask; e) forming a second mask exposing a portion of the source regions; f) implanting the exposed portions of the source region with n⁺ dopant ions; and g) removing the second source mask; wherein the edge of the first source mask does not coincide with a (SGE) stacked gate edge adjacent the shared source regions.

Claims 1-4 depend from independent claim 1 and recite further features of the present invention.

Lim does not does not anticipate nor render obvious a method for manufacturing a flash memory having a lightly doped source region “wherein the source mask does not coincide with the SGE adjacent the shared source regions” as is recited in claim 1. Lim only shows a conventional flash memory cell fabrication methodology. Lim does not teach a source mask that is not coincident with a SGE. Nowhere in Lim is a source mask having the attributes of the source mask defined in Applicants Claim 1 shown or suggested.

Applicants “Background of the Invention” does not overcome the shortcomings of Lim. Applicants “Background of the Invention” only describes conventional flash memory device fabrication techniques. It should be noted that the Applicants “Background of the Invention” does not teach a source mask that is not coincident with a SGE. In fact, Nowhere in the Applicants “Background of the Invention” is a source mask having the attributes of the source mask defined in Applicants Claim 1 shown or suggested. Consequently, Lim and the Applicants “Background of the Invention” either alone or in combination do not show are suggest the Applicants invention as is set forth in Claim 1.

Therefore, Applicants respectfully submit that Lim and the Applicants “Background of the Invention” either alone or in combination do not anticipate or suggest the present claimed invention as recited in Claim 1 and, as such, Claim 1 traverses the

Examiner's basis for rejection under 35 U.S.C. §103. Accordingly, Applicants respectfully submit that Claim 1 is in condition for allowance. In addition, Applicants respectfully submit that Lim and the Applicants "Background of the Invention" either alone or in combination do not anticipate or suggest the present invention as is recited in Claims 2-4 which depend from Claim 1, and that Claims 2-4 are also in condition for allowance as being dependent on an allowable base claim.

Claim 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lim (6,265,265) view of The Background of the Invention. Applicants have reviewed the cited reference and respectfully submit that the present invention as recited in claim 1 is neither shown nor suggested by Lim (6,265,265) view of The Background of the Invention.

The examiner is respectfully directed to independent claim 5 which recites that an embodiment of the present invention is directed to a method for manufacturing a flash memory device having a lightly doped source region comprising:

- a) forming multiple gates on a substrate defining drain regions and source regions associated with each of the multiple gates; b) forming a source mask exposing the source regions; c) implanting the exposed source regions with n⁺ dopant ions; and d) removing the source mask; wherein the edge of the first source mask does not coincide with a (SGE) stacked gate edge adjacent the shared source regions.

Claims 6 and 7 depend from independent claim 5 and recite further features of the present invention.

Lim does not anticipate nor render obvious a method for manufacturing a flash memory having a lightly doped source region “wherein the source mask does not coincide with the SGE adjacent the shared source regions” as is recited in claim 5. Lim only shows a conventional flash memory cell fabrication methodology. Lim does not teach a source mask that is not coincident with a SGE. Nowhere in Lim is a source mask having the attributes of the source mask defined in Applicants Claim 5 shown or suggested.

Applicants “Background of the Invention” does not overcome the shortcomings of Lim. Applicants “Background of the Invention” only describes conventional flash memory device fabrication techniques. It should be noted that the Applicants “Background of the Invention” does not teach a source mask that is not coincident with a SGE. In fact, Nowhere in the Applicants “Background of the Invention” is a source mask having the attributes of the source mask defined in Applicants Claim 5 shown or suggested. Consequently, Lim and the Applicants “Background of the Invention” either alone or in combination do not show or suggest the Applicants invention as is set forth in the Claims.

Therefore, Applicants respectfully submit that Lim and the Applicants “Background of the Invention” either alone or in combination do not anticipate nor suggest the present claimed invention as recited in Claim 5 and, as such, Claim 5 traverses the Examiner’s basis for rejection under 35 U.S.C. §103. Accordingly, Applicants respectfully submit that Claim 5 is in condition for allowance. In addition,

Applicants respectfully submit that Lim and the Applicants “Background of the Invention” either alone or in combination do not anticipate nor suggest the present invention as is recited in Claims 6 and 7 which depend from Claim 5, and that Claims 6 and 7 are also in condition for allowance as being dependent on an allowable base claim.

SUMMARY

In view of the foregoing amendments and remarks, Applicants respectfully submit that the pending claims are in condition for allowance. Applicants respectfully request reconsideration of the application and allowance of the pending claims.

If the Examiner determines the prompt allowance of these claims could be facilitated by a telephone conference, the examiner is invited to contact Reginald A. Ratliff at (408) 938-9060.

Respectfully submitted,

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MARKED-UP VERSION TO SHOW CHANGES

IN THE CLAIMS

Please amend the Claims as follows:

1. (Amended) A method of manufacturing a flash memory Electrically-Erasable Programmable Read Only Memory (EEPROM) device having a lightly-doped source region near the critical gate region and a heavily-doped source region away from the critical gate region wherein the lateral diffusion of the source dopants is decreased and having low V_{ss} resistance, and wherein the EEPROM includes a multitude of field effect transistor memory cells each having a source, drain, a floating gate, a control gate and a substrate, the method comprising:

- (a) forming multiple gates on a substrate defining drain regions and source regions associated with each of the multiple gates;
- b) forming a first source mask exposing the source regions and portions of the gates;
- c) implanting the exposed source regions with n dopant ions;
- d) removing the first source mask;
- e) forming a second mask exposing a portion of the source regions;
- f) implanting the exposed portions of the source region with n⁺ dopant ions; and
- g) removing the second source mask[.];

wherein the edge of the first source mask does not coincide with a (SGE) stacked gate edge adjacent the shared source regions.

5. (Amended) A method of manufacturing a flash memory Electrically-Erasable Programmable Read Only Memory (EEPROM) device having a lightly-doped source region near the critical gate region and a heavily-doped source region away from the critical gate region wherein the lateral diffusion of the source dopants is decreased and having low V_{ss} resistance, and wherein the EEPROM includes a multitude of field effect transistor memory cells each having a source, drain, a floating gate, a control gate and a substrate, the method comprising:

- a) forming multiple gates on a substrate defining drain regions and source regions associated with each of the multiple gates;
- b) forming a source mask exposing the source regions;
- c) implanting the exposed source regions with n⁺ dopant ions; and
- d) removing the source mask[.];

wherein the edge of the first source mask does not coincide with a (SGE) stacked gate edge adjacent the shared source regions.